

DC-to-DC Converter Control Circuit

LM34063AQ8

Description

The LM34063AQ8 is a monolithic control circuit containing the primary functions required for DC-to-DC converters. This device consists of an internal temperature compensated reference, comparator, control- led duty cycle oscillator with an active current limit circuit, driver and high current output switch.

Features

- 3V to 40V Input Voltage Operation
- Internal 1.6A Peak Current Switch
- Internal $\pm 1.8\%$ Reference
- Low Quiescent Current at 1.6mA
- Frequency Operation from 100Hz~100KHz
- Current Limiting

Applications

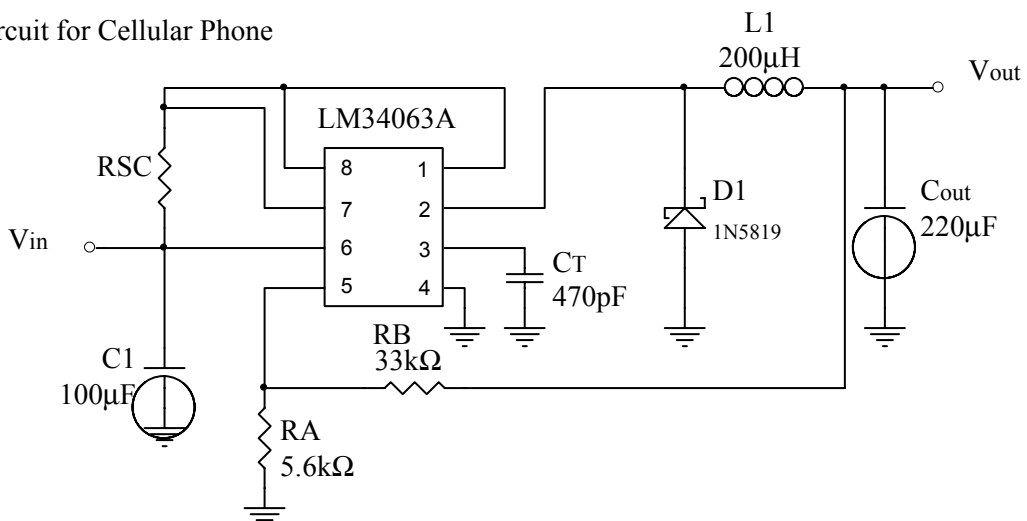
- Saver for Cellular Phone
- DC-DC Converter Module

Ordering Information

Device	Package	Shipping
LM34063AQ8	SOP-8 (Pb-free lead plating package)	2500 pcs / tape & reel, 3000 pcs/tape & reel

Typical Application Circuit

Fig1.Saver Circuit for Cellular Phone





Pin Connections

	Pin1:Switch Collector	Pin5:Comparator Inverting Input
	Pin2:Switch Emitter	Pin6:Vcc
	Pin3:Timing Capacitor	Pin7:Ipk Sense
	Pin4:Gnd	Pin8:Driver Collector

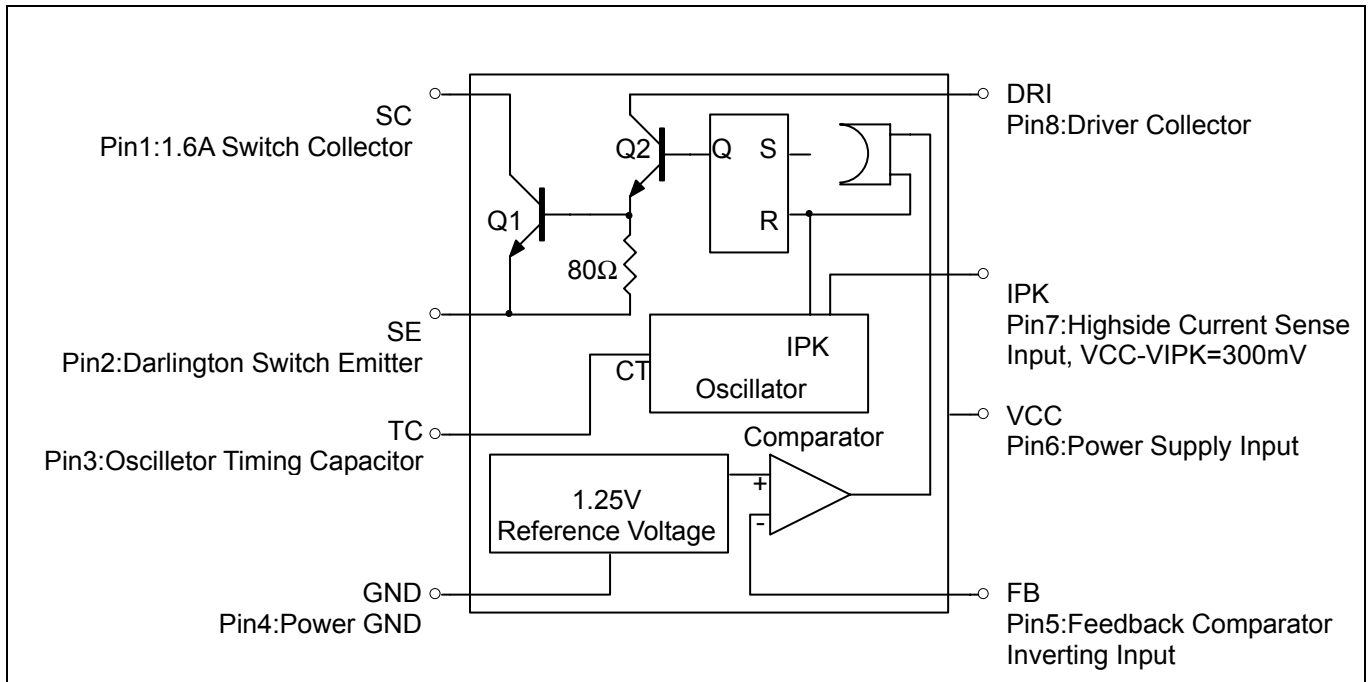
Absolute Maximum Rating

Supply Voltage	40 V
Comparator Input Voltage Range	-0.3 V ~ 40 V
Switch Collector Voltage	40 V
Switch Emitter Voltage	40 V
Switch Collector to Emitter Voltage	40 V
Driver Collector Voltage	40 V
Switch Current	1.6A
Power Dissipation @ Ta=25°C.....	625 mW
Thermal Resistance Junction to Air.....	160 °C / W
Operating Junction Temperature.....	125 °C
Operating Ambient Temperature Range.....	0 ~ 70 °C
Storage Temperature Range.....	-40 °C ~ 125 °C

Electrical Characteristics (Vcc=5V, Ta=25°C, unless otherwise specified)

Parameter	Test Condition	Symbol	Min.	Typ.	Max.	Unit
<i>Oscillator</i>						
Frequency	Vpin 5=0V, CT=1nF	fosc	30	38	45	kHz
Charging Current	5.0V≤VCC≤40V	Ichg	30	38	45	μA
Discharge Current	5.0V≤VCC≤40V	Idischg	180	240	290	μA
Voltage Amplitude	Pin3	VOSC	-	0.6	-	V
Discharge to Charge Current Ratio	VIPK(Sence) =VCC	IDischg/Ichg	5.2	6.5	7.5	-
Current Limit Sense Voltage	IChg=Idischg	VIPK(Sence)	250	300	350	mV
<i>Output Switch</i>						
Saturation Voltage, Darlington Connection	ISW=1.0A, VC(Driver)=VC(Switch)	VCE(Sat)	-	1.0	1.3	V
Saturation Voltage	ISW=1.0A, IC(Driver)=50mA (Forced β ≈ 20)	VCE(Sat)	-	0.45	0.8	V
DC Current Gain	ISW=1.0A, VCE=5.0V	hFE	50	75	-	-
Collector Off-State Current	VCE=40V	ICC(Off)	-	0.01	100	μA
<i>Comparator</i>						
Threshold Voltage		VTH	1.225	1.250	1.275	V
	0°C≤Ta≤70°C		1.210	-	1.290	
Threshold Voltage Line Regulation	3.0V≤VCC≤40V	Regline	-	1.4	5	mV
Input Bias Current	VIN=0V	IIB	-	-20	-400	nA
Supply Current	VIPK(Sence)=VCC VPin5>VFB, 5.0V≤VCC≤40V CT=1nF, Pin2=Gnd Remaining pins open	ICC	-	1.6	4	mA

Block Diagram



Application Information

Design Formula Table

Calculation	Step-Down	Step-Up	Voltage-Inverting
ton / toff	$\frac{V_{out} + V_F}{V_{in(min)} - V_{sat} - V_{out}}$	$\frac{V_{out} + V_F - V_{in(min)}}{V_{in(min)} - V_{sat}}$	$\frac{ V_{out} + V_F}{V_{in} - V_{sat}}$
(ton + toff) max	1/Fmin	1/Fmin	1/Fmin
CT	$4 * 10^{-5} * t_{on}$	$4 * 10^{-5} * t_{on}$	$4 * 10^{-5} * t_{on}$
IC(switch)	2 * Iout(max)	2 * Iout(max) * (ton + toff / toff)	2 * Iout(max) * (ton + toff / toff)
RS	0.3 / IC(switch)	0.3 / IC(switch)	0.3 / IC(switch)
L(min)	$\frac{(V_{in(min)} - V_{sat} - V_{out})}{I_{out(max)} * t_{on(max)}}$	$\frac{(V_{in(min)} - V_{sat})}{I_{out(max)} * t_{on(max)}}$	$\frac{(V_{in(min)} - V_{sat})}{I_{out(max)} * t_{on(max)}}$
CO	$\frac{I_{C(switch)} * (ton + toff)}{8 * V_{Ripple(P-P)}}$	$\frac{I_{out} * t_{on}}{V_{Ripple(P-P)}}$	$\frac{I_{out} * t_{on}}{V_{Ripple(P-P)}}$

Vsat : Saturation voltage of the output switch.

VF : Forward voltage drop of the ringback rectifier.

The following power supply characteristics must be chosen :

Vin : Nominal input voltage.

Vout : Desired output voltage. $|V_{out}| = 1.25 * (1 + R_B / R_A)$

Iout - Desired output current

Fmin : Minimum desired output switching frequency at the selected values for Vin and Iout.

VRipple(P-P) : Desired peak to peak output ripple voltage in practice, the calculated value will need to be increased due to the capacitor equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly effect the line and load regulation.

Application Information (Continued)

Fig.2 Step-Up Converter

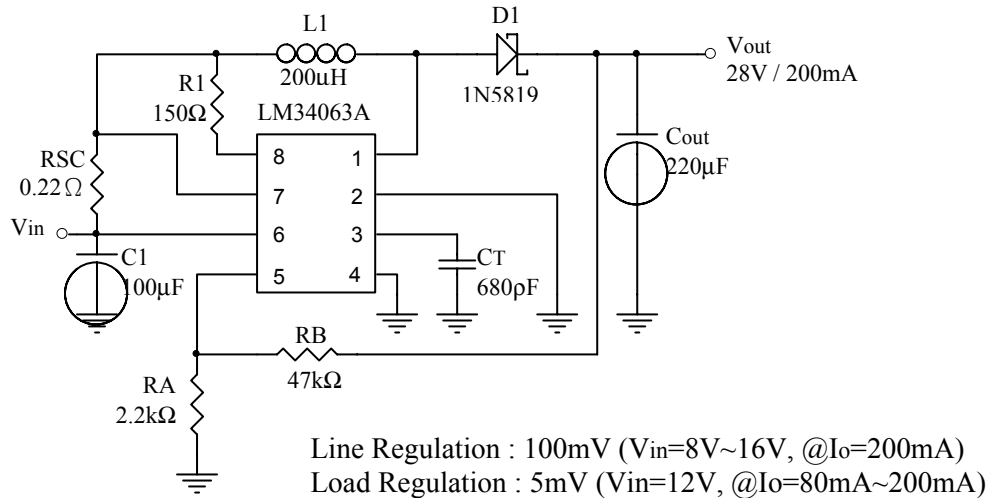


Fig.3 Step-Up Converter With External NPN Switch

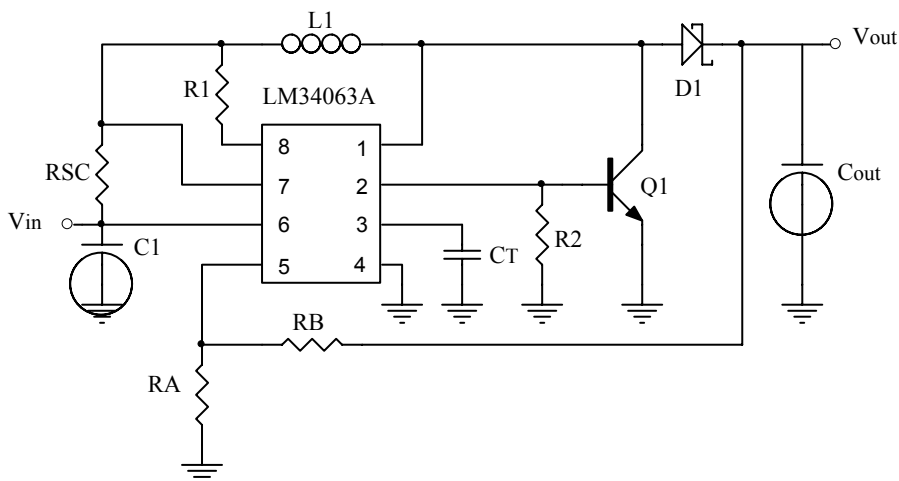
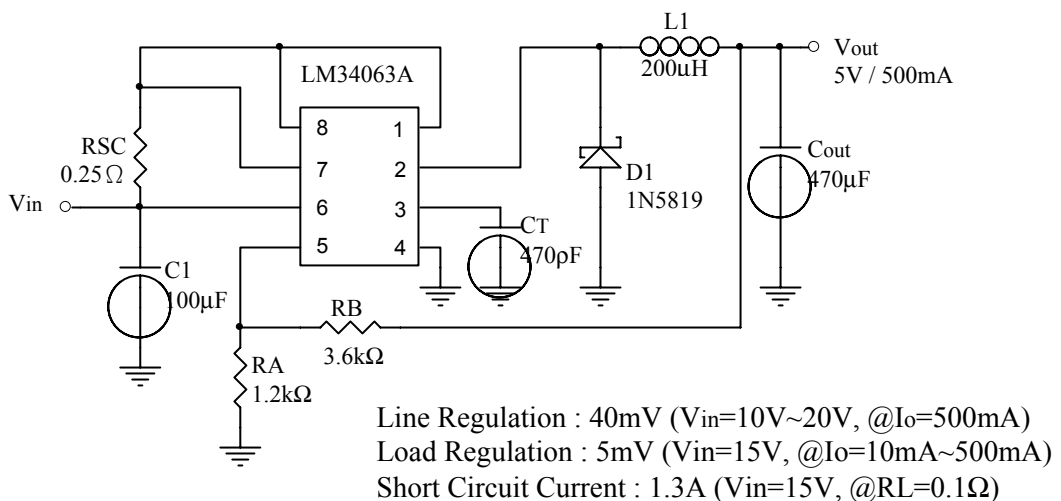


Fig.4 Step-Down Converter



Application Information (Continued)

Fig.5 Step-Down Converter With External PNP Saturation Switch

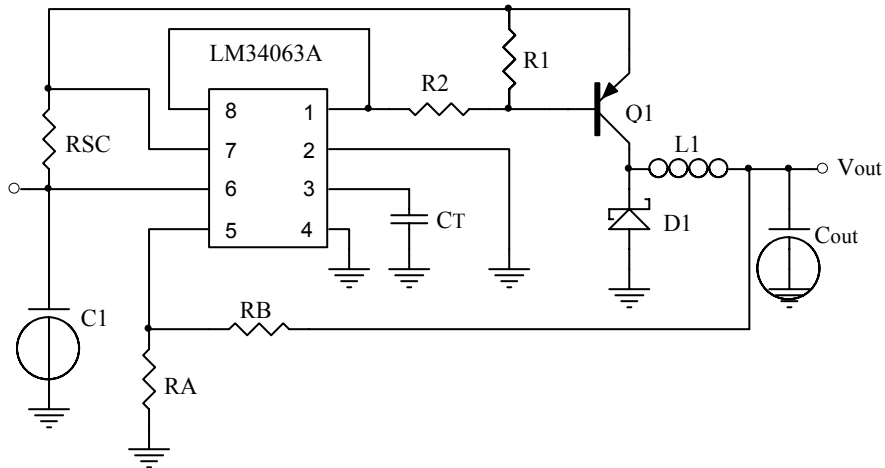


Fig.6 Voltage Inverting Converter

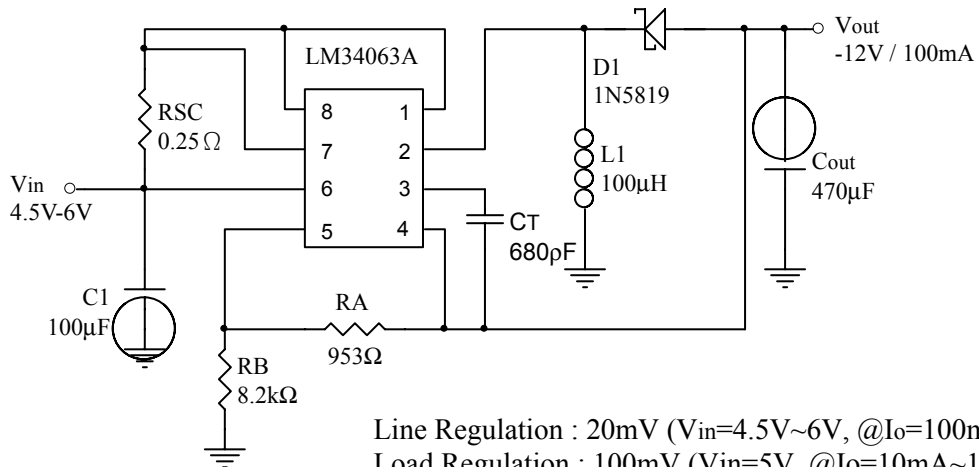
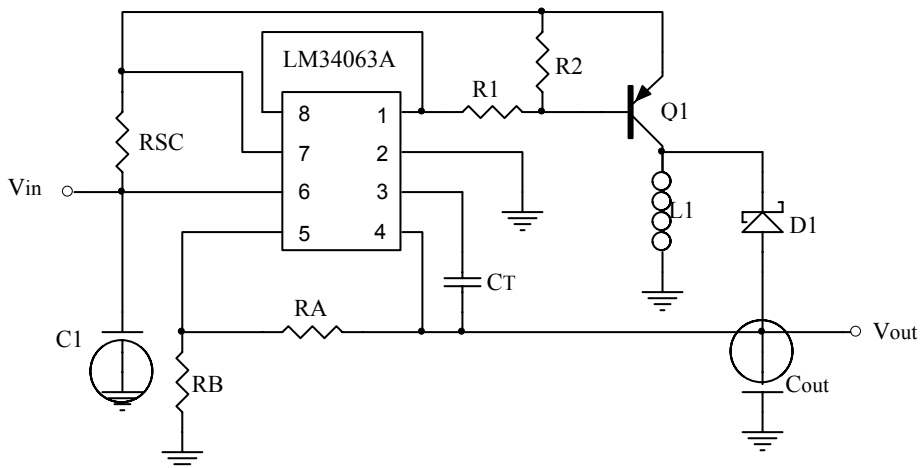
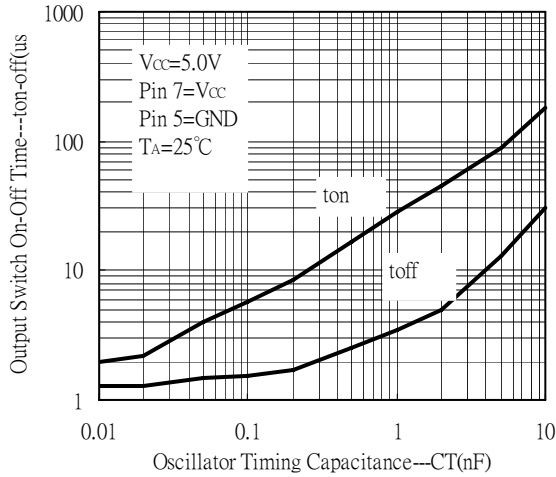


Fig.7 Voltage Inverting Converter With External PNP Saturation Switch

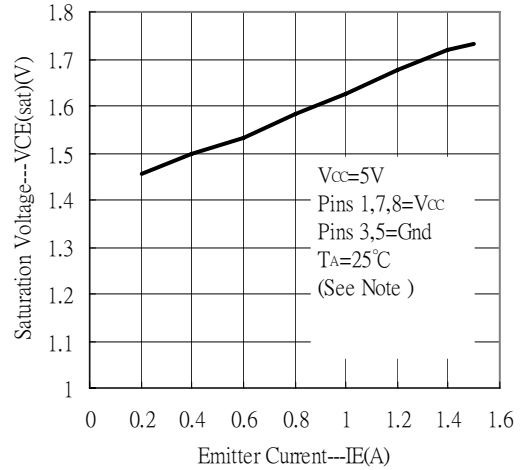


Characteristic Curves

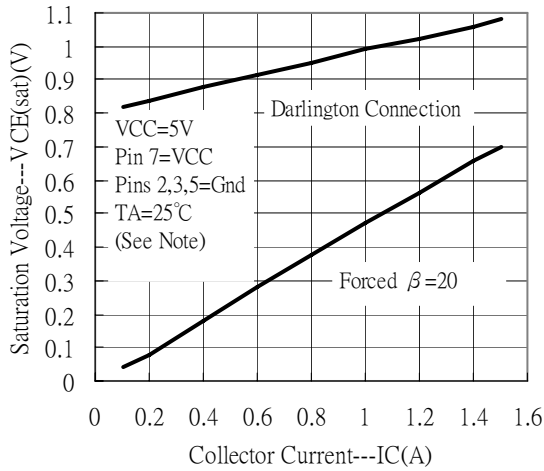
Output Switch On-Off Time vs Oscillator Timing Capacitance



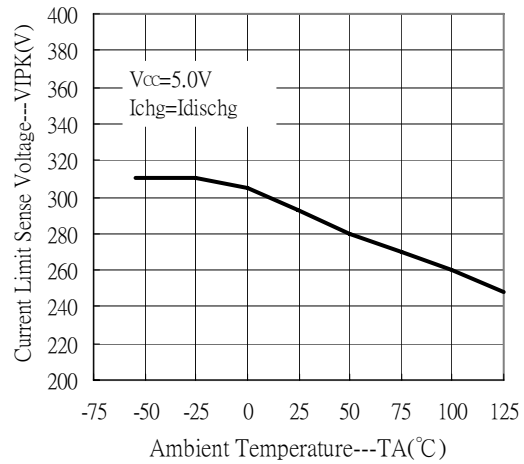
Emitter Follower Configuration Output Saturation Voltage vs Emitter Current



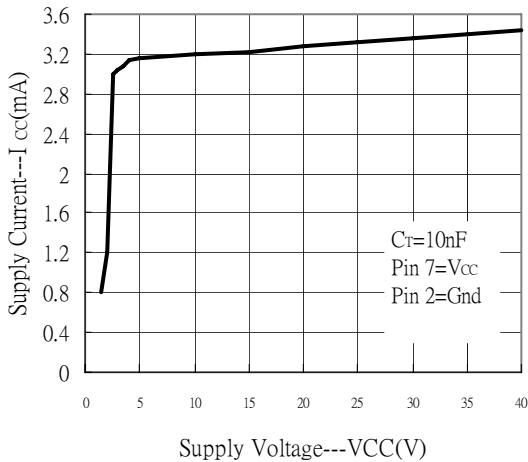
Common Emitter Configuration Output Switch Saturation Voltage vs Collector Current



Current Limit Sense Voltage vs Temperature

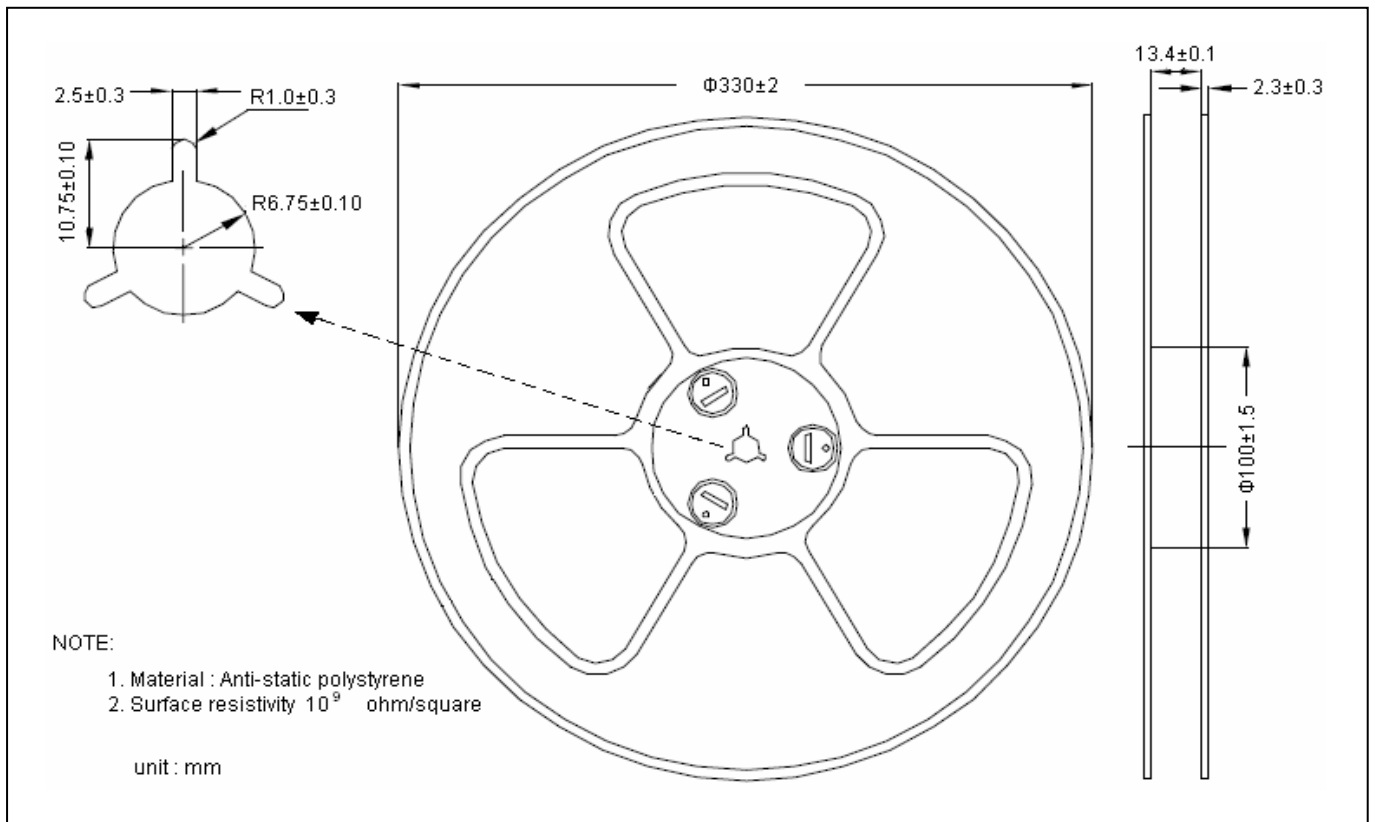


Standby Supply Current vs Supply Voltage

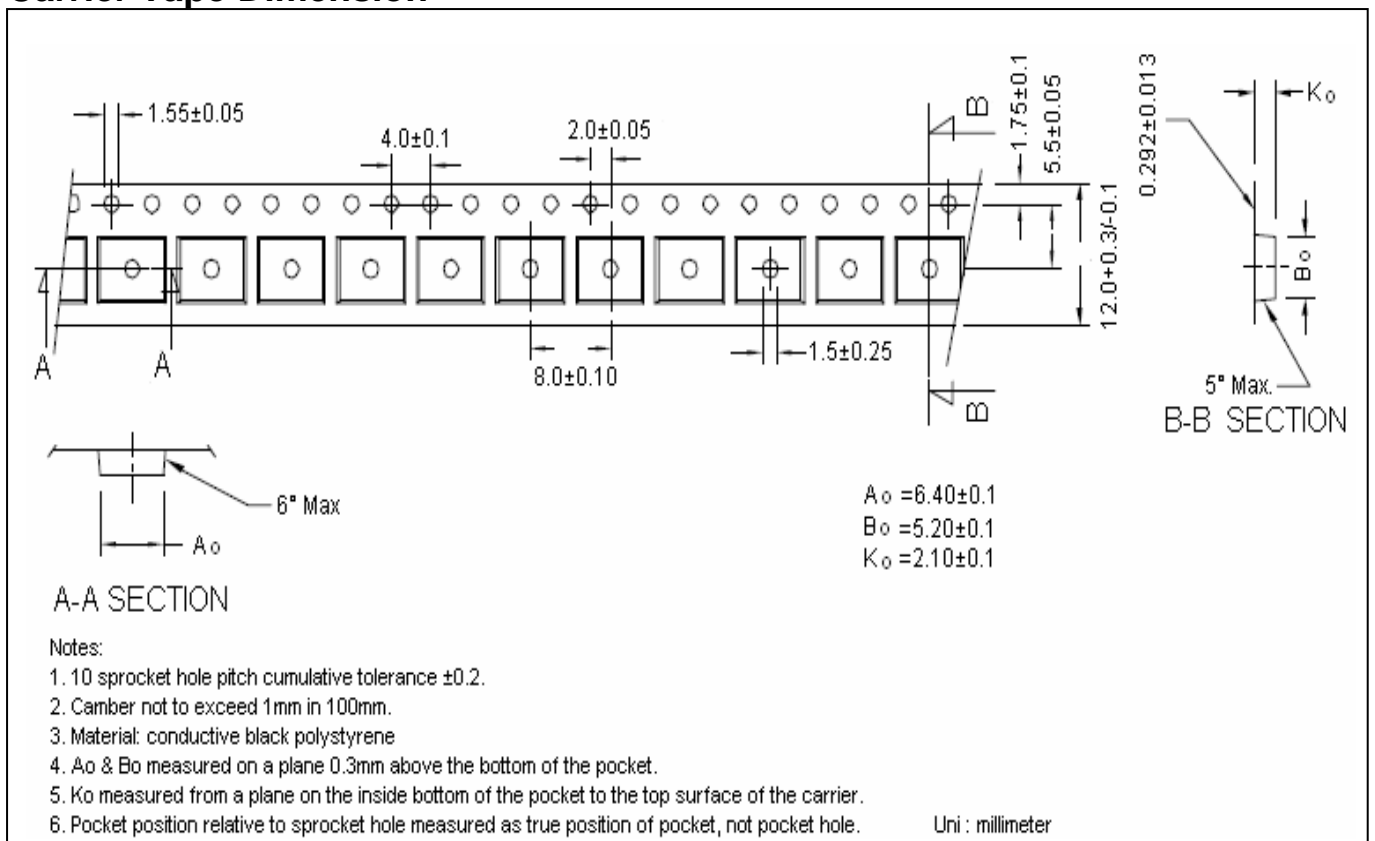


Note: Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.

Reel Dimension



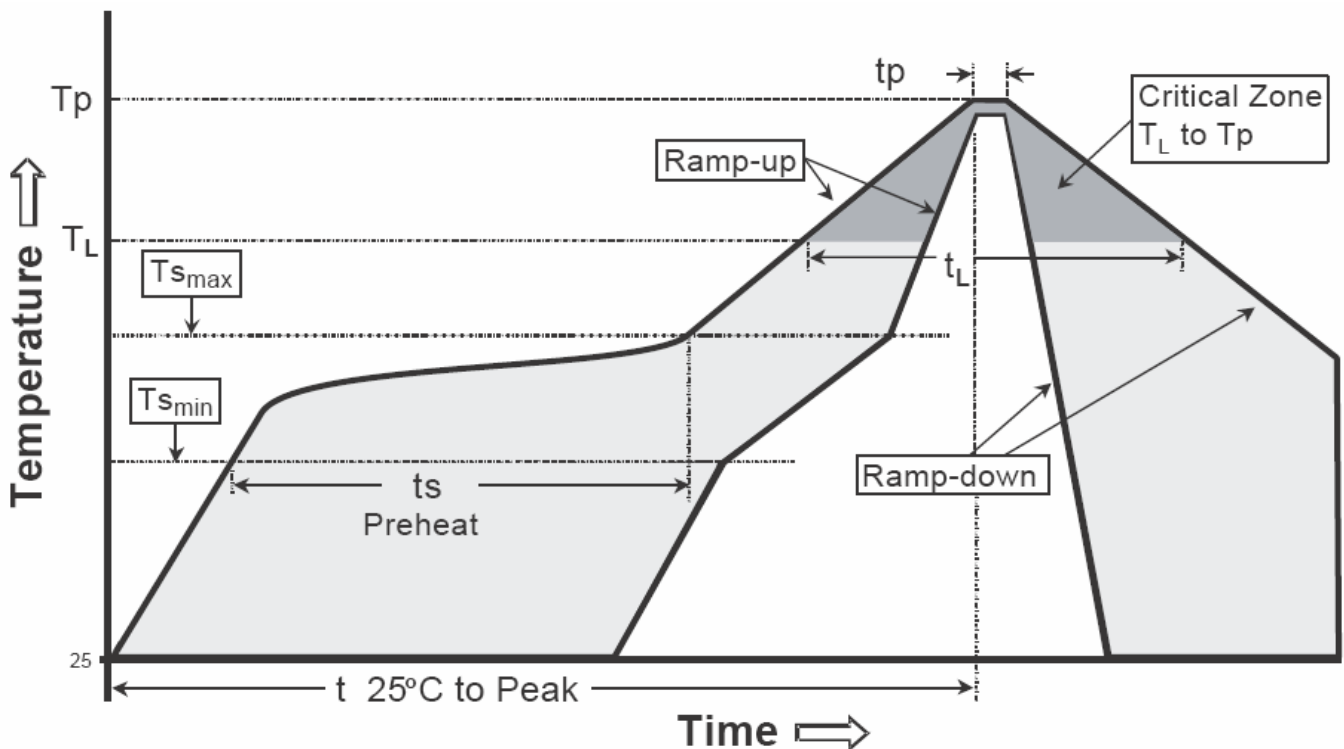
Carrier Tape Dimension



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

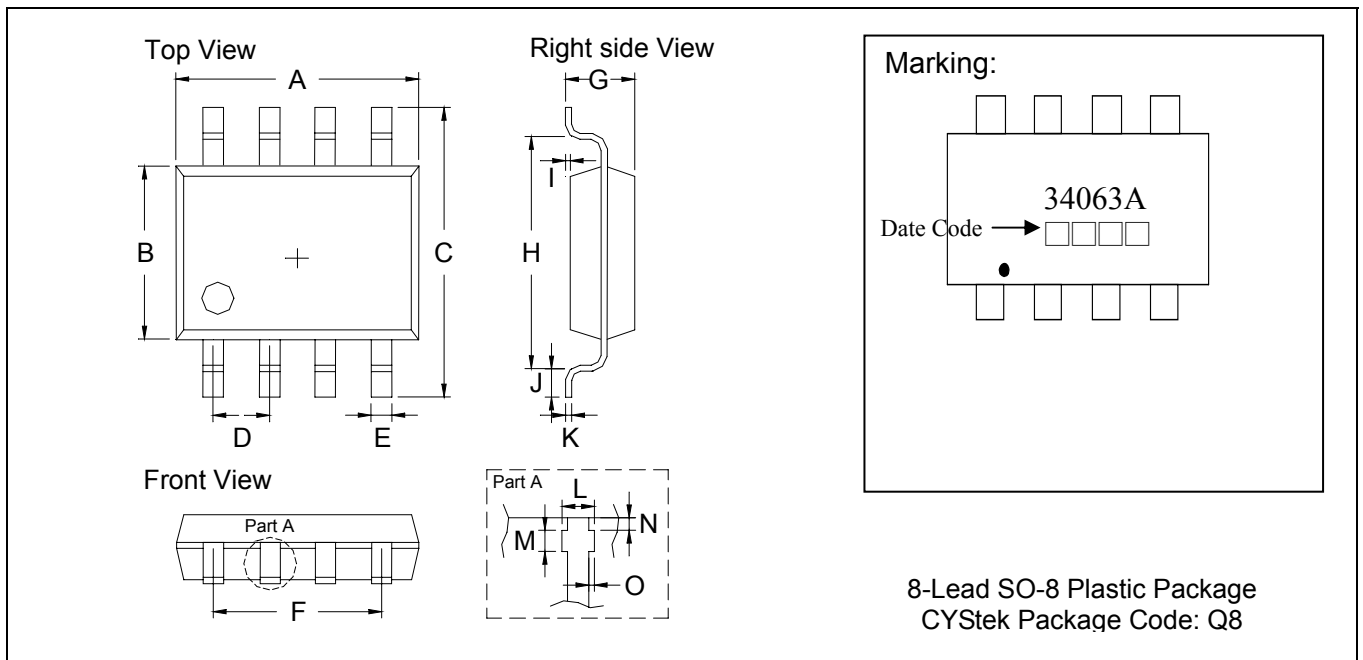
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(Ts min)	100°C	150°C
-Temperature Max(Ts max)	150°C	200°C
-Time(ts min to ts max)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (Tl)	183°C	217°C
- Time (tl)	60-150 seconds	60-150 seconds
Peak Temperature(Tp)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

SO-8 Dimension



*: Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.1909	0.2007	4.85	5.10	I	0.0019	0.0078	0.05	0.20
B	0.1515	0.1555	3.85	3.95	J	0.0118	0.0275	0.30	0.70
C	0.2283	0.2441	5.80	6.20	K	0.0074	0.0098	0.19	0.25
D	0.0480	0.0519	1.22	1.32	L	0.0145	0.0204	0.37	0.52
E	0.0145	0.0185	0.37	0.47	M	0.0118	0.0197	0.30	0.50
F	0.1472	0.1527	3.74	3.88	N	0.0031	0.0051	0.08	0.13
G	0.0570	0.0649	1.45	1.65	O	0.0000	0.0059	0.00	0.15
H	0.1889	0.2007	4.80	5.10					

Notes: 1. Controlling dimension: millimeters.
 2. Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3. If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

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